Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 256 x 16, 512 x 16, 1,024 x 16

IDT72105
IDT72115
IDT72125

FEATURES:

- 25ns parallel port access time, 35ns cycle time
- 45MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the FL/DIR pin
- Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full
- Dual-Port zero fall-through architecture
- Available in 28-pin 300 mil plastic DIP and 28-pin SOIC
- Industrial temperature range (–40°C to +85°C)

DESCRIPTION:

The IDT72105/72115/72125s are very high-speed, low-power,dedicated, parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port with 256, 512 and 1,024 word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

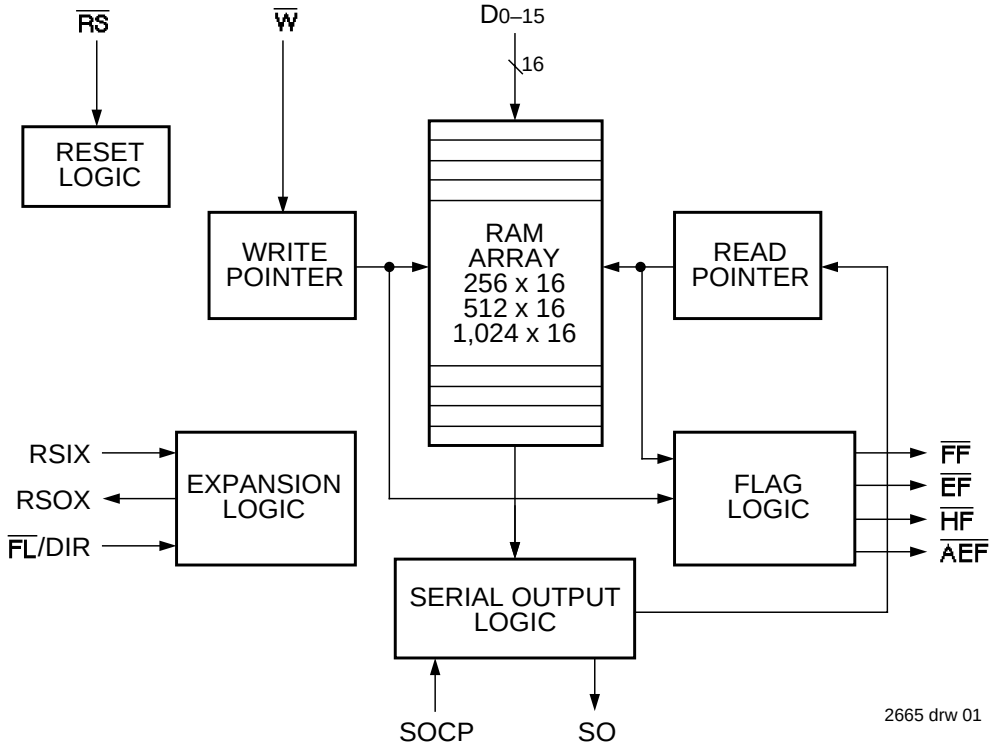
Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

The IDT72105/72115/72125 are fabricated using IDT's leading edge, submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of Mil-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



STATUS FLAGS

Number of Words in FIFO						
IDT72105	IDT72115	IDT72125	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1–31	1–63	1–127	H	L	H	H
32–128	64–256	128–512	H	H	H	H
129–224	257–448	513–896	H	H	L	H
225–255	449–511	897–1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE: 2665 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.0	—	—	V
V_{IL}(1)	Input LOW Voltage	—	—	0.8	V
T_A	Operating Temperature	-40	—	+85	°C

NOTE: 2665 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	IDT72105 IDT72115 IDT72125 Industrial Min.	Typ.	Max.	Unit
I_{LI} (1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA(3)	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA(4)	—	—	0.4	V
I_{CC1}(5)	Active Power Supply Current	—	50	100	mA
I_{CC2}(5,6,7)	Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = VIH; SOCP = VIL)	—	4	8	mA
I_{CC3}(5,6,7)	Power Down Current	—	1	6	mA

NOTES: 2665 tbl 05

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. SOCP = V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. For SO, I_{OUT} = –4mA.
4. For SO, I_{OUT} = 16mA.
5. Tested with outputs open (I_{OUT} = 0).
6. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = V_{CC} - 0.2V; SOCP = 0.2V; all other inputs = V_{CC} - 0.2.
7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5V±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Figure	INDUSTRIAL 72105L25 72115L25 72125L25 Min.	Max.	INDUSTRIAL 72105L50 72115L50 72125L50 Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	—	28.5	—	15	MHz
t_{SOCP}	Serial Shift Frequency	—	—	50	—	40	MHz
PARALLEL INPUT TIMINGS							
t_{WC}	Write Cycle Time	2	35	—	65	—	ns
t_{WPW}	Write Pulse Width	2	25	—	50	—	ns
t_{WR}	Write Recovery Time	2	10	—	15	—	ns
t_{DS}	Data Set-up Time	2	12	—	15	—	ns
t_{DH}	Data Hold Time	2	0	—	2	—	ns
t_{WEF}	Write High to $\overline{EF}$ HIGH	5, 6	—	35	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ LOW	4, 7	—	35	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ HIGH	7	25	—	50	—	ns
SERIAL OUTPUT TIMINGS							
t_{SOCP}	Serial Clock Cycle Time	3	20	—	25	—	ns
t_{SOCW}	Serial Clock Width HIGH/LOW	3	8	—	10	—	ns
t_{SOPD}	SOCP Rising Edge to SO Valid Data	3	—	14	—	15	ns
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	3	3	14	3	15	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	3	3	14	3	15	ns
t_{SOCEF}	SOCP Rising Edge to $\overline{EF}$ LOW	5, 6	—	35	—	45	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ HIGH	4, 7	—	35	—	45	ns
t_{SOCF}	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
t_{REFSO}	SOCP Delay After $\overline{EF}$ HIGH	6	35	—	65	—	ns
RESET TIMINGS							
t_{RSC}	Reset Cycle Time	1	35	—	65	—	ns
t_{RS}	Reset Pulse Width	1	25	—	50	—	ns
t_{RSS}	Reset Set-up Time	1	25	—	50	—	ns
t_{RSR}	Reset Recovery Time	1	10	—	15	—	ns
EXPANSION MODE TIMINGS							
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	8	—	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	2	—	ns
t_{DIRS}	DIR Set-up Time to SOCP Rising Edge	9	10	—	12	—	ns
t_{DIRH}	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	ns
t_{SOXD1}	SOCP Rising Edge to RSOX Rising Edge	9	—	15	—	17	ns
t_{SOXD2}	SOCP Rising Edge to RSOX Falling Edge	9	—	15	—	17	ns
t_{SIXS}	RSIX Set-up Time to SOCP Rising Edge	9	5	—	8	—	ns
t_{SIXPW}	RSIX Pulse Width	9	10	—	15	—	ns

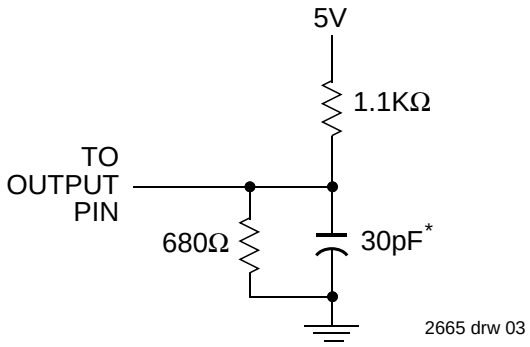
NOTE:
1. Values guaranteed by design.

2665 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. Characterized values, not currently tested.

2665 tbl 08

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

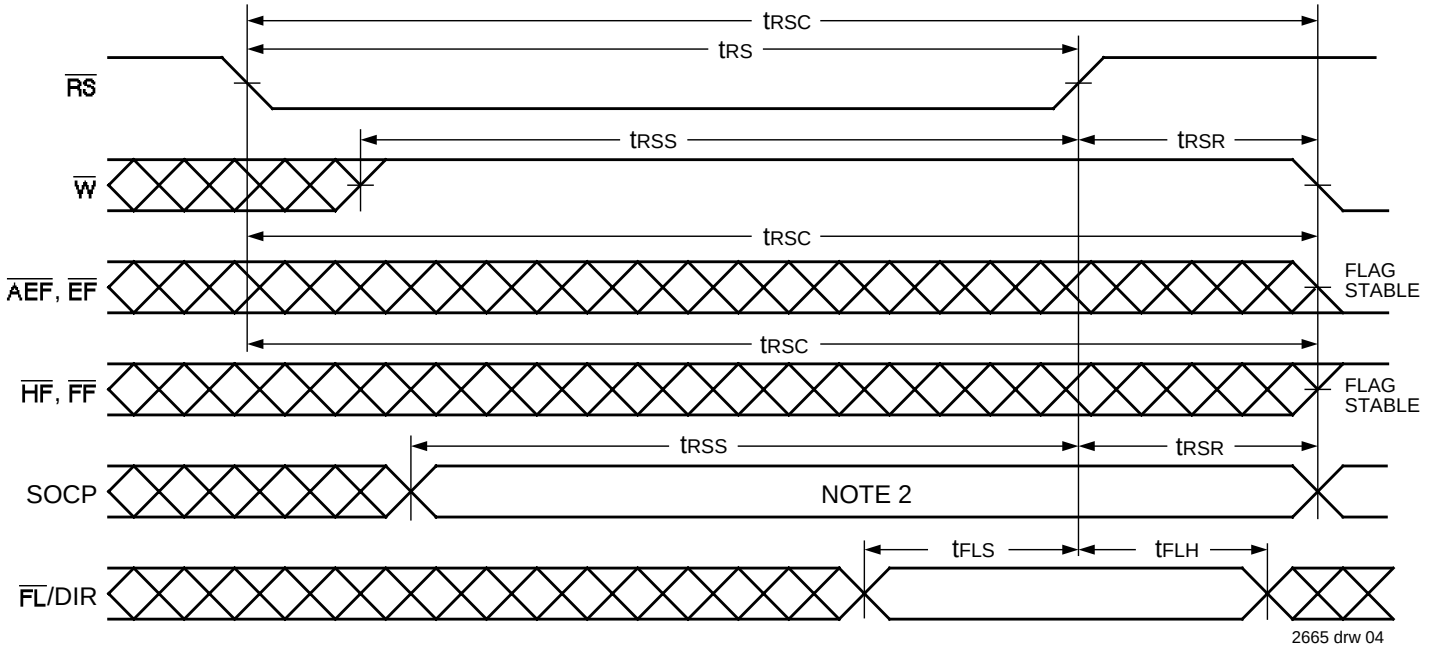
The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is internally inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. SOCP should be in the steady LOW or HIGH during t_{RSS}. The first LOW-HIGH (or HIGH-LOW) transition can begin after t_{RSR}.

Figure 1. Reset

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half- Full Flag Output, $\overline{FF}$ = Full Flag Output.

2665 tbl 10

Table 2. Reset and First Load Truth Table–Width/Depth Compound Expansion Mode

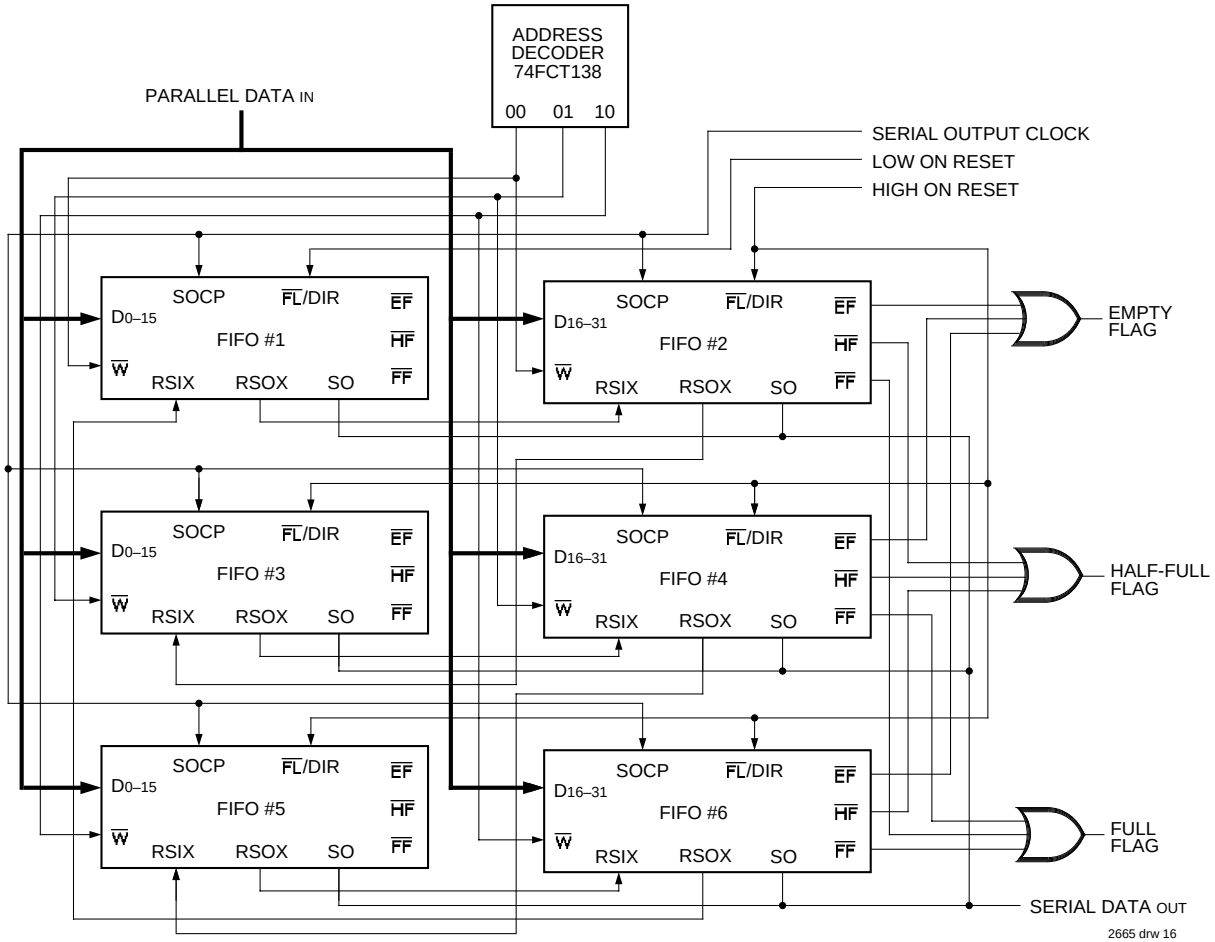


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

ORDERING INFORMATION